

Form PTO-1449 (REV. 8-83)	U.S. DEPARTMENT OF COMM PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. NVID-001/000US	SERIAL NO. 09/056,656
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT: Curtis Priem et al.	
		FILING DATE April 7, 1998	GROUP 2776

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
<i>m</i>	P1	4,586,038	04/29/86	Sims et al.	340	729	12/12/83
	P2	4,615,013	09/30/86	Yan et al.	364	521	08/02/83
	P3	4,727,365	02/23/88	Bunker et al.	340	728	05/21/86
	P4	4,821,212	04/11/89	Heartz	364	521	08/08/84
	P5	4,905,164	02/27/90	Chandler et al.	364	518	12/19/86
	P6	4,924,414	05/08/90	Ueda	364	522	09/24/87
	P7	4,935,879	06/19/90	Ueda	364	522	08/05/88
	P8	4,945,495	07/31/90	Ueda	364	518	10/20/88
	P9	4,945,500	07/31/90	Deering	364	522	11/20/89
	P10	5,029,225	07/02/91	Ueda	382	28	09/20/89
	P11	5,097,427	03/17/92	Lathrop et al.	395	130	03/26/91
	P12	5,157,388	10/20/92	Kohn	340	800	04/02/91
	P13	5,179,638	01/12/93	Dawson et al.	395	125	04/26/90
	P14	5,185,856	02/09/93	Alcorn et al.	395	130	03/16/90
	P15	5,222,205	06/22/93	Larson et al.	395	130	03/16/90
	P16	5,392,393	02/21/95	Deering	395	162	06/04/93

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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
<i>m</i>	P17	5,224,208	06/29/93	Miller, Jr. et al.	395	125	03/16/90
	P18	5,255,360	10/19/93	Peaslee et al.	395	162	09/14/90
	P19	5,493,643	02/20/96	Soderberg et al.	395	162	02/20/96
	P20	5,517,611	05/14/96	Deering	395	163	07/24/95
	P21	5,519,823	05/21/96	Barkans	395	143	01/11/95
	P22	5,548,709	08/20/96	Hannah et al.	395	164	03/07/94
	P23	5,706,481	01/06/98	Hannah et al.	395	519	05/22/96
	P24	5,760,783	06/02/98	Migdal et al.	345	430	11/06/95
<i>↓</i>	P25	5,987,567	11/16/99	Rivard et al.	711	118	09/30/96

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
<i>m</i>	F1	0 319 165 A2	06/07/89	Europe	G06F15	72	X	
	F2	0 447 222 A2	09/18/91	Europe	G06F15	72	X	
	F3	0 454 129 A2	10/30/91	Europe	G06F15	72	X	
	F4	1-114990	05/08/89	Japan	G06F15	72 and 60	X (Abs.)	
<i>↓</i>	F5	5-298456	11/12/93	Japan	G06F15	72	X (Abs.)	

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							YES	NO
m	F6	5-307610	11/19/93	Japan	G06F15	72	X (Abs.)	
	F7	6-36039	02/10/94	Japan	G06F15	72	X (Abs.)	
	F8	63-80375	04/11/88	Japan	G06F15	72	X (Abs.)	
↓	F9	WO 90/00774	01/25/90	WIPO	G06F15	3	X	
					G06F20	153		

OTHER PUBLICATIONS (including Author, Title, Date, Pertinent Pages, Etc.)

m	D1	Alan Norton et al.; "Clamping: A Method of Antialiasing Textured Surfaces by Bandwidth Limiting in Object Space," <u>Computer Graphics</u> , Vol. 16, No. 3 (July, 1982), pp. 1-8.
	D2	Nobuyuki Yagi et al.; "A Programmable Video Signal Multi-Processor for HDTV Signals," <u>IEEE</u> , (1993), pp. 1754-1757.
	D3	Graham J. Dunnett et al.; "The Image Chip for High Performance 3D Rendering," <u>IEEE</u> , (November, 1992) pp. 41-52.
	D4	James E. Dudgeon, et al; "Algorithms for Graphics Texture Mapping," <u>IEEE</u> , (1991), pp. 613-617.
	D5	Akira Yamazaki et al.; "A Concurrent Operating CDRAM for Low Cost Multi-Media," <u>1993 Symposium on VLSI Circuits - Digest of Technical Papers</u> , (May 19-21, 1993), Kyoto, Japan, pp. 61-62.
	D6	Dave Bursky; "Combination DRAM-SRAM Removes Secondary Caches," <u>Electronic Design</u> , (January 23, 1992), pp. 39-40, 42-43.
	D7	John Poulton et al.; "Breaking the Frame-Buffer Bottleneck with Logic Enhanced Memories," <u>IEEE Computer Graphics & Applications</u> , (November, 1992), pp. 65-74.
	D8	David A. Patterson et al.; "Computer Architecture a Quantitative Approach," ©1990 Morgan Kaufmann Publishers, Inc. [ISBN 1-55860-069-8], pp. 425-432.
	D9	Stephen A. Ward et al.; "Computation Structures," (Second Printing), ©1990 MIT Press [ISBN 0-262-23139-5], pp. 476-478.
↓	D10	Loring Wirrel; "Intel's i860 Takes High-End Graphics Lead," <u>Electronic Engineering Times</u> (March 26, 1990) pp. 134, 136.

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	D11	M. Agate et al.; "A Multiple Application Graphics Integrated Circuit - MAGIC," <u>Eurographics '86</u> , (©Eurographics Association 1986), pp. 67-77.					
	D12	Michael Deering et al.; "The Triangle Processor and Normal Vector Shader: A VLSI System for High Performance Graphics," <u>Computer Graphics</u> , Vol. 22, No. 4, (August, 1988), pp. 21-30.					
	D13	Paul Winser et al.; "Architectures for Mass Market 3D Displays," <u>Eurographics '88</u> , (©Eurographics Association), pp. 273-283.					
	D14	David Kirk et al.; "The Rendering Architecture of the DN10000VS," <u>Computer Graphics</u> , Vol. 24, No. 4 (August 1990), pp. 299-307.					
	D15	Forrest Norrod et al.; "An Advanced VLSI Chip Set for Very-High-Speed Graphics Rendering," <u>Conference Proceedings - NCGA '91 Conference & Exposition</u> , (April 22-25, 1991, Chicago), pp. 1-10.					
	D16	A.M. Kovalev et al.; "Computer Systems for Image Analysis and Synthesis - Increasing the Quality of Texture Mapping onto Planar Surfaces," <u>Optoelectronics, Instrumentation and Data Processing</u> , No. 3, 1991, pp. 3-10.					
	D17	Adrian Sfarti et al.; "Method for Filling Shaded, Textured z-Buffered Polygons," 13 pages. (undated)					
	D18	Intel Computers, "i860™ 64-Bit Microprocessor Simulator and Debugger Reference Manual," Version 3, January 1990, 167 pages.					
	D19	Larry J. Thayer; "Advanced Workstation-Graphics Hardware Features," <u>Conference Proceedings - NCGA 1990</u> , (pp.309-315)					

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